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(54) **ORGANIC LIGHT EMITTING DISPLAY AND METHOD OF DRIVING THE SAME**

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(57) **ABSTRACT**

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An organic light emitting display and a method of driving the same, in which a driving frequency is lowered and at the same time a production cost is reduced. The organic light emitting display includes: a display region divided into a left part and a right part; a first data driver adapted to supply a data signal to data lines of the left part; a second data driver adapted to supply the data signal to data lines of the right part; and first and second memory groups wherein, when one of the first and second memory groups stores data to be supplied to the left and right parts therein, another one of the first and second memory groups supplies data to the first and second drivers, and wherein, when one of the first and second memory groups receives a reading signal in parallel, another one of the first and second memory groups receives a writing signal in series. With this configuration, the frequency of a clock included in a reading signal supplied to a line memory is lowered, thereby reducing a production cost.

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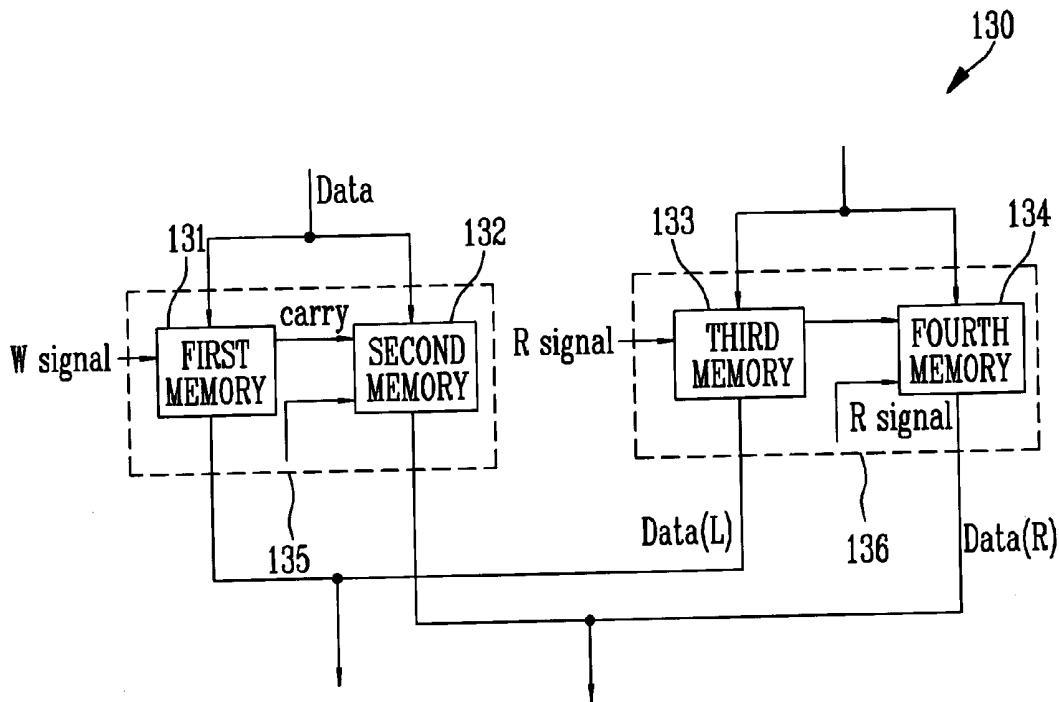


FIG. 1
(PRIOR ART)

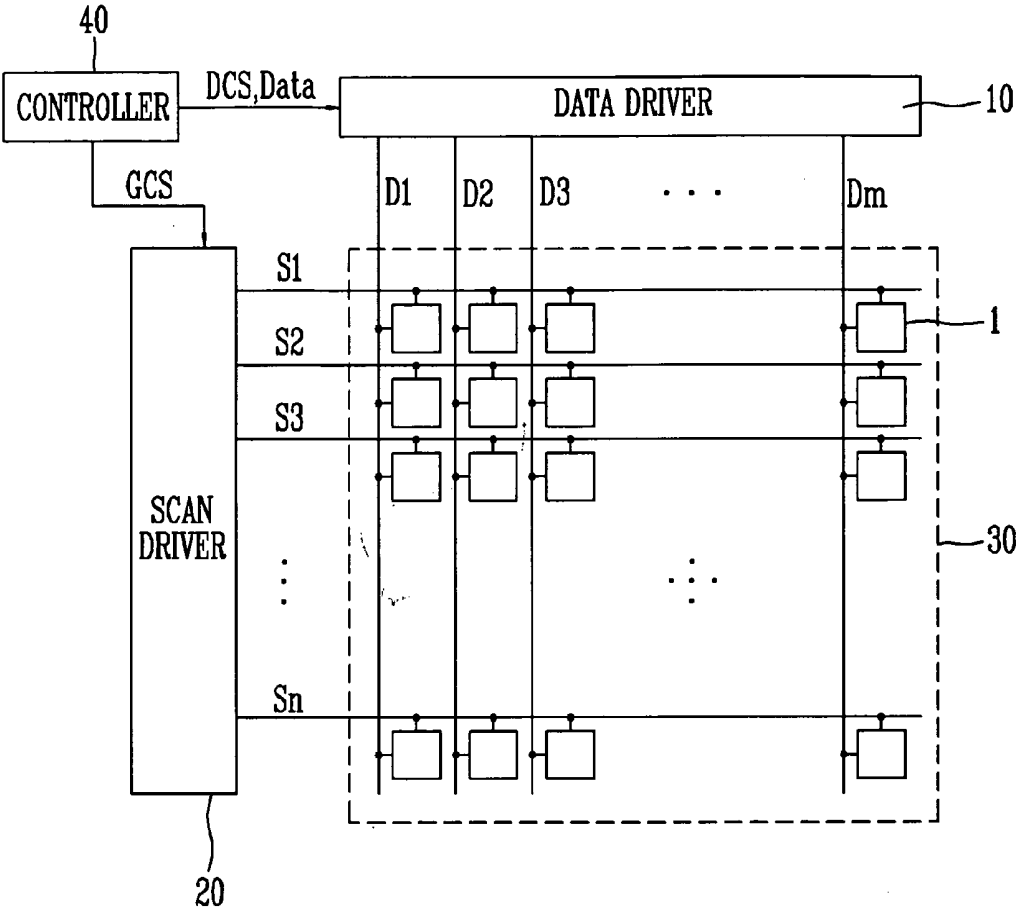


FIG. 2A
(PRIOR ART)

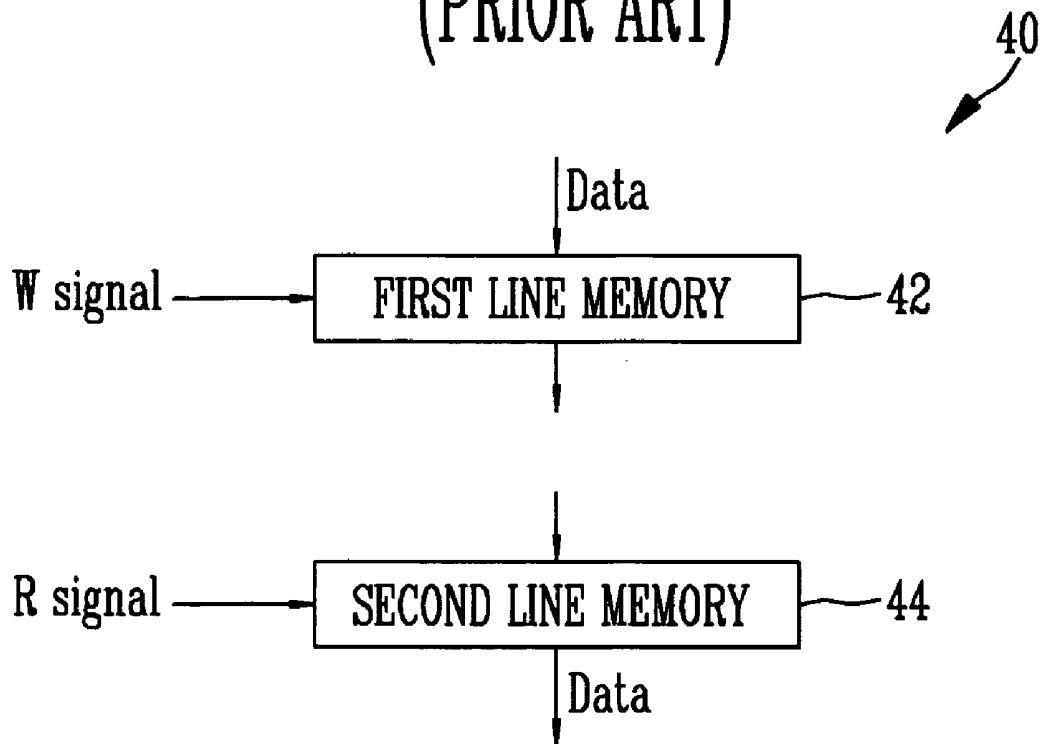


FIG. 2B
(PRIOR ART)

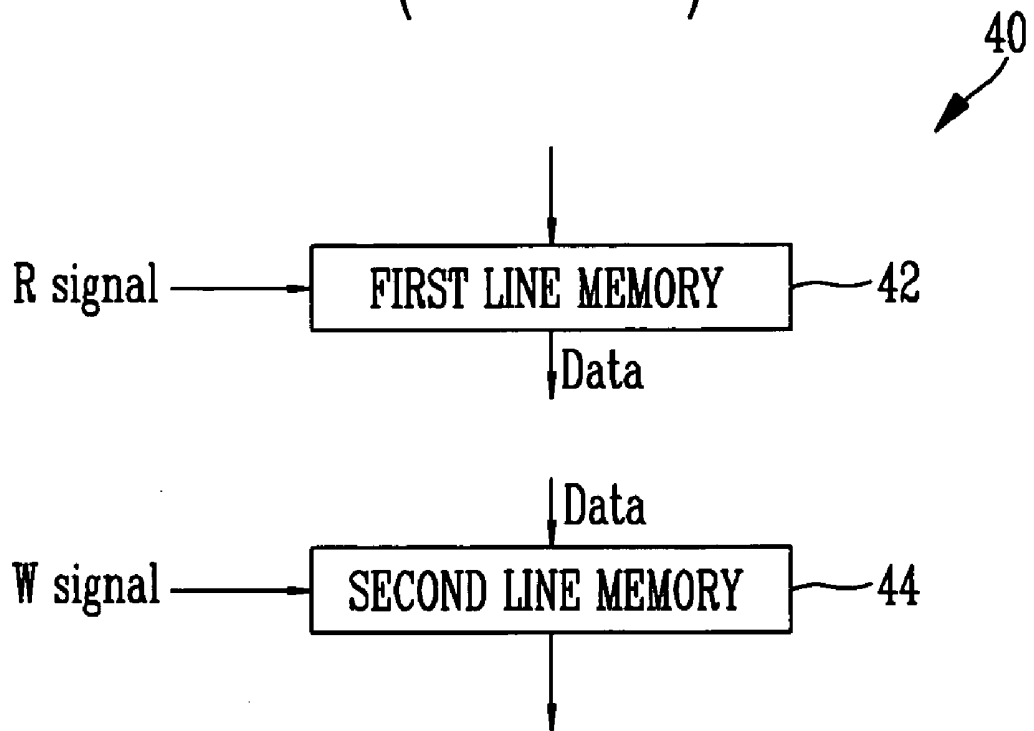


FIG. 3
(PRIOR ART)

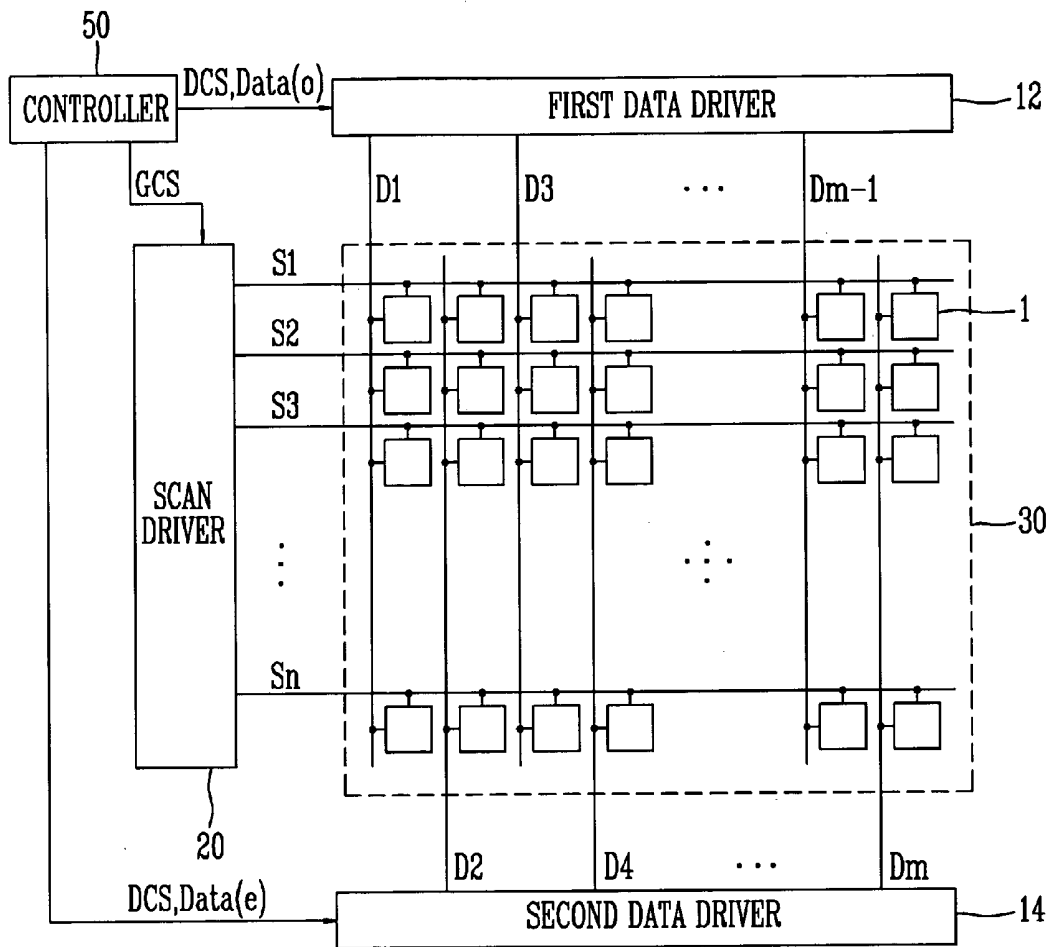


FIG. 4A
(PRIOR ART)

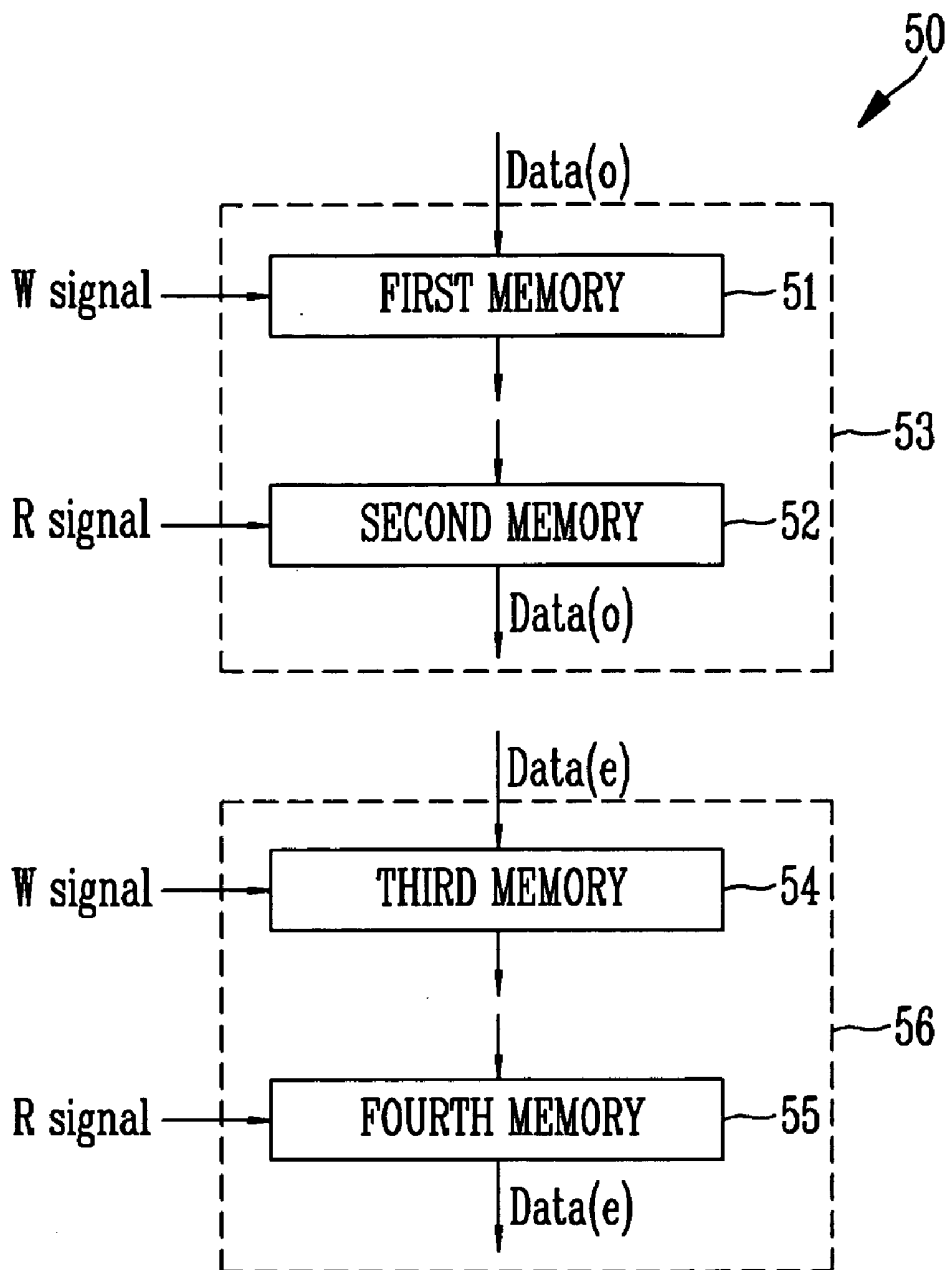


FIG. 4B
(PRIOR ART)

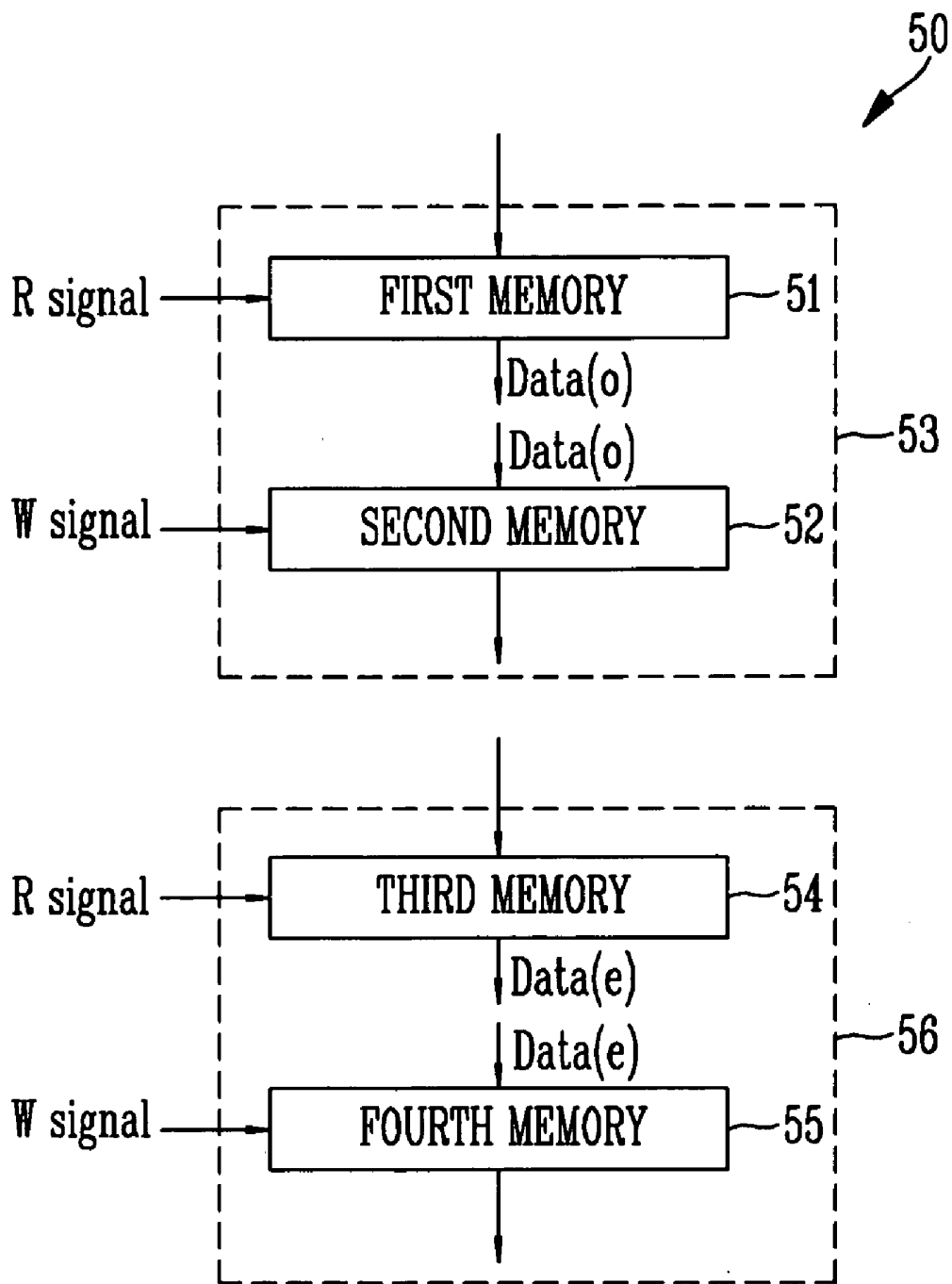


FIG. 5

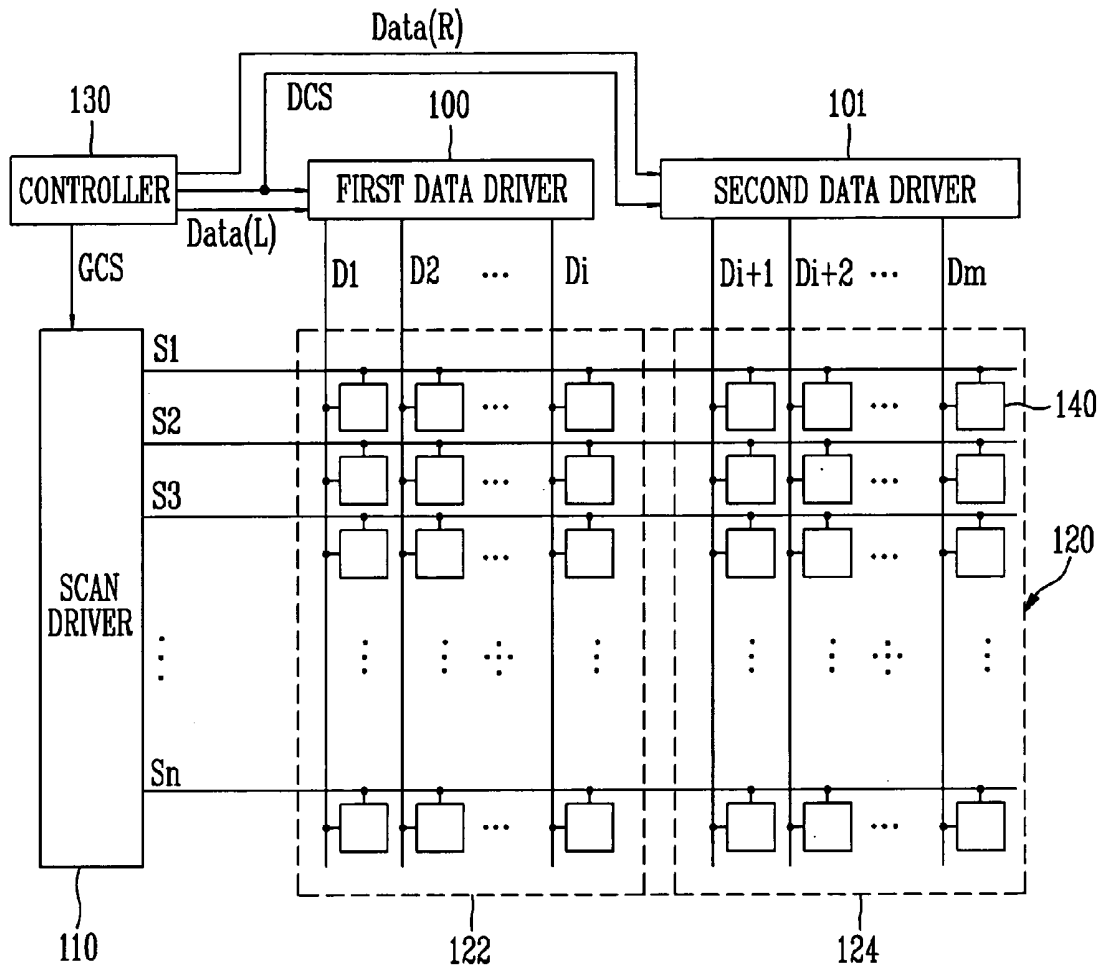


FIG. 6A

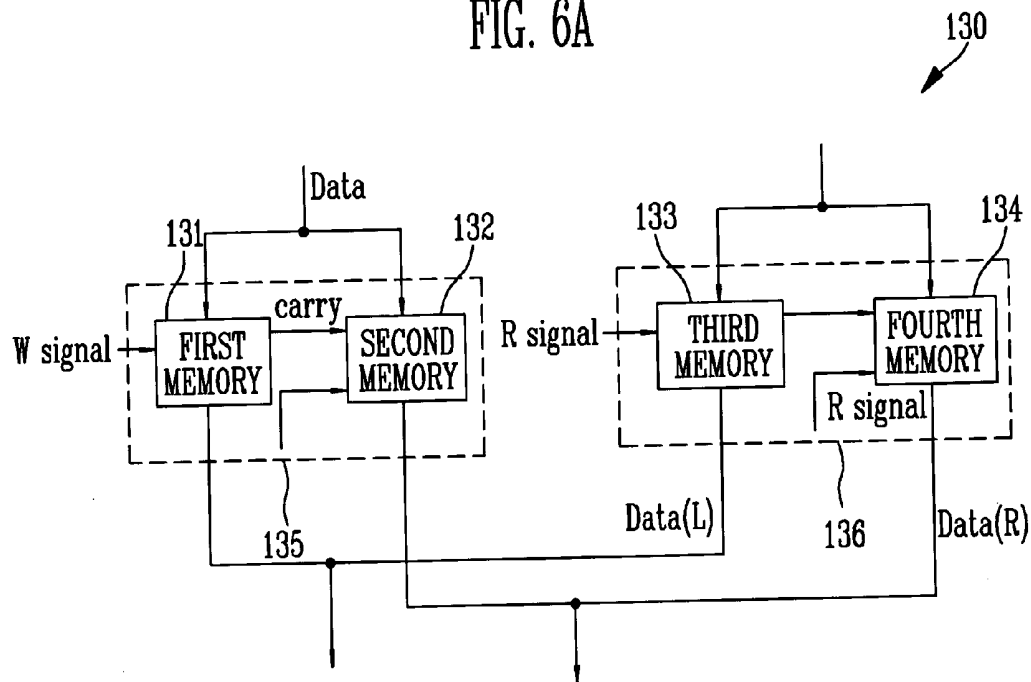


FIG. 6B

130

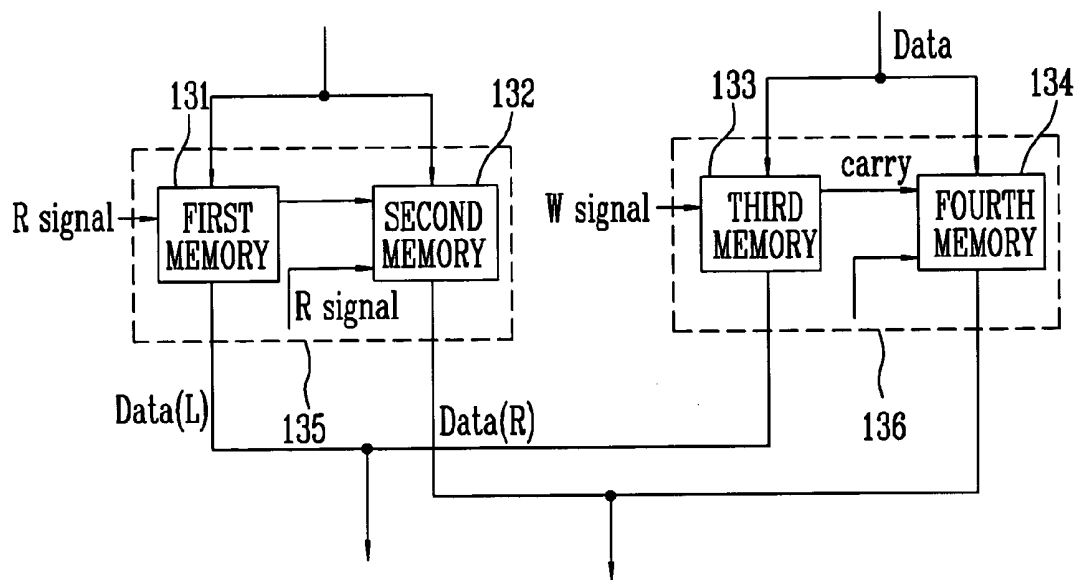


FIG. 7

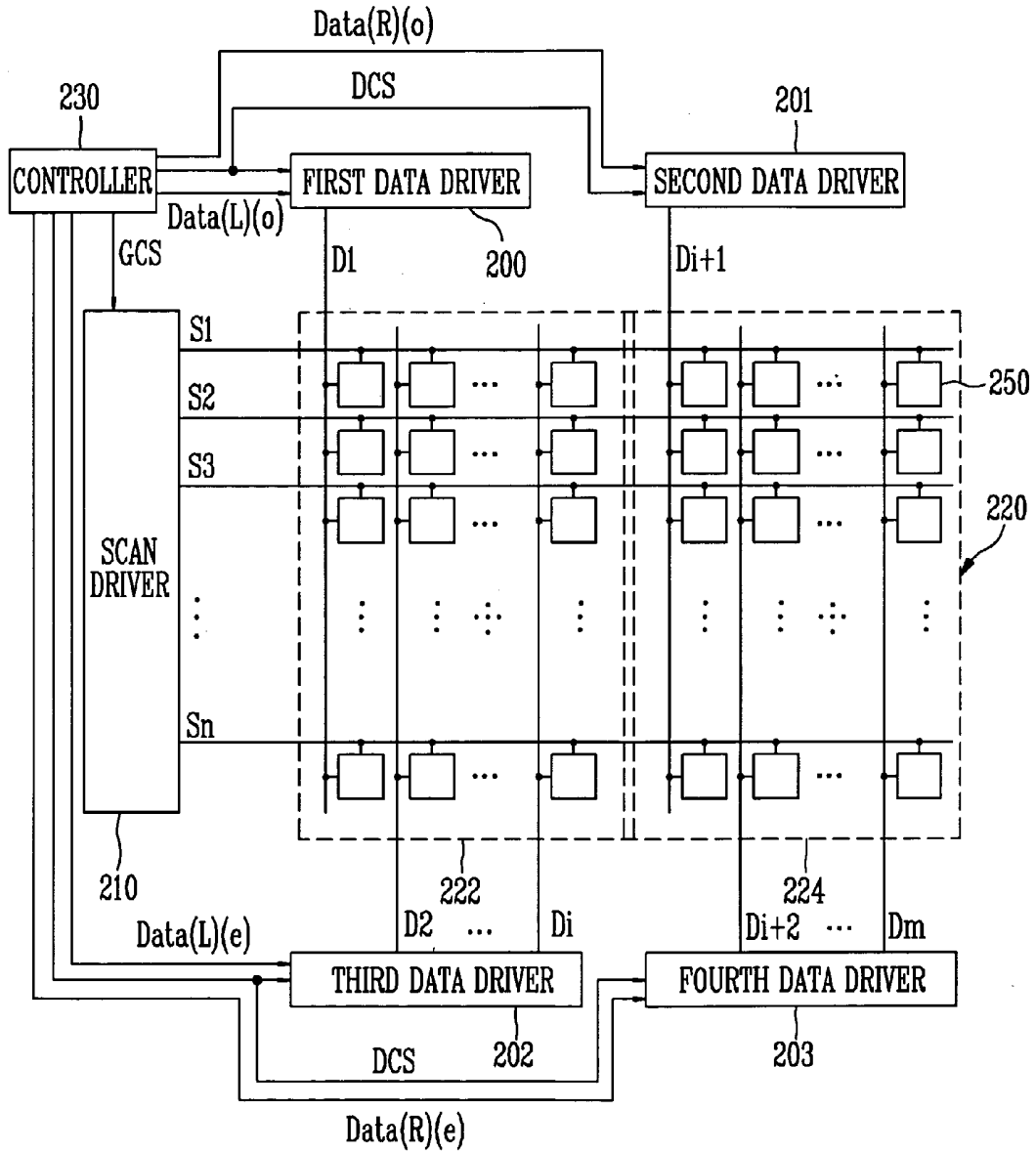


FIG. 8A

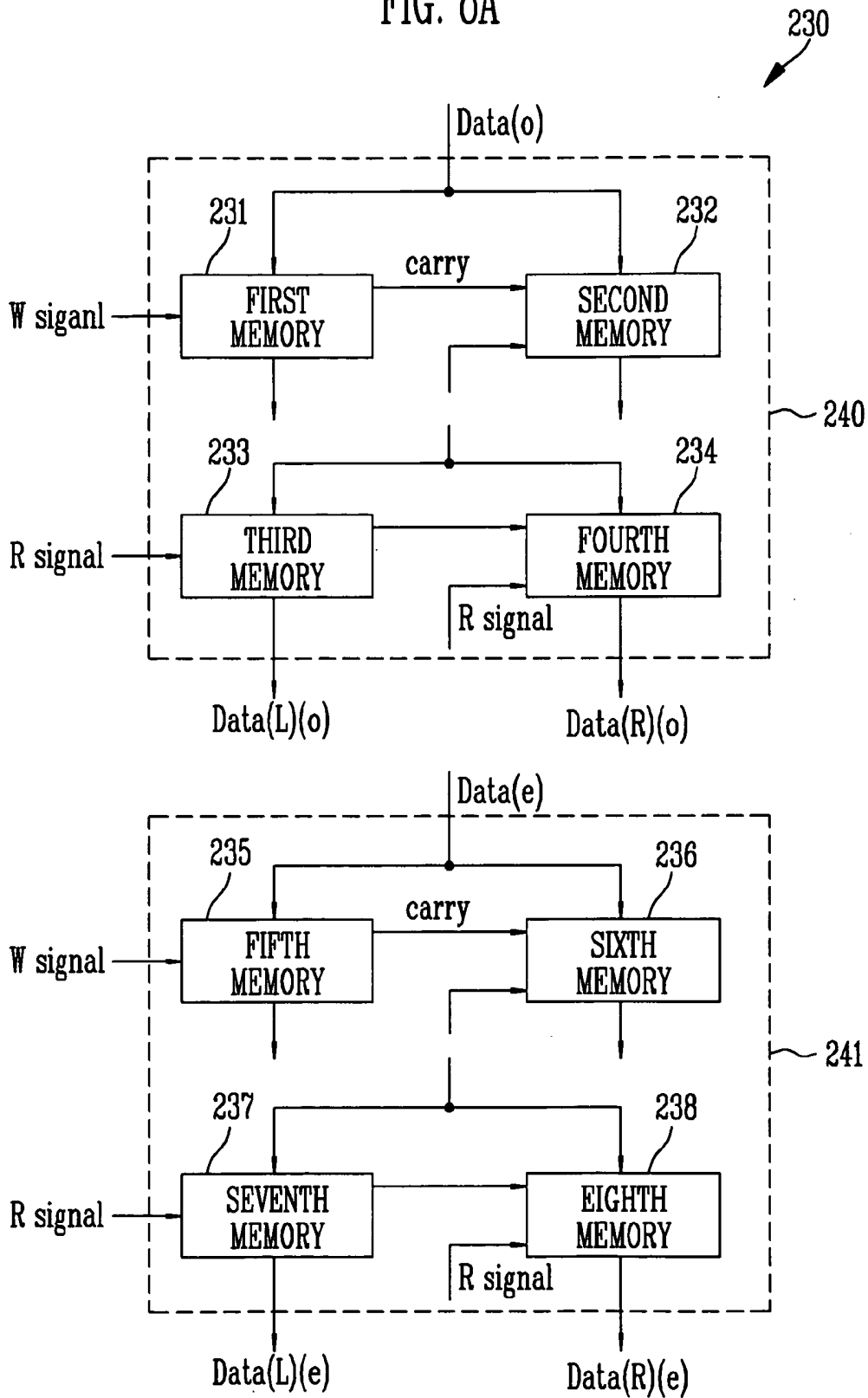
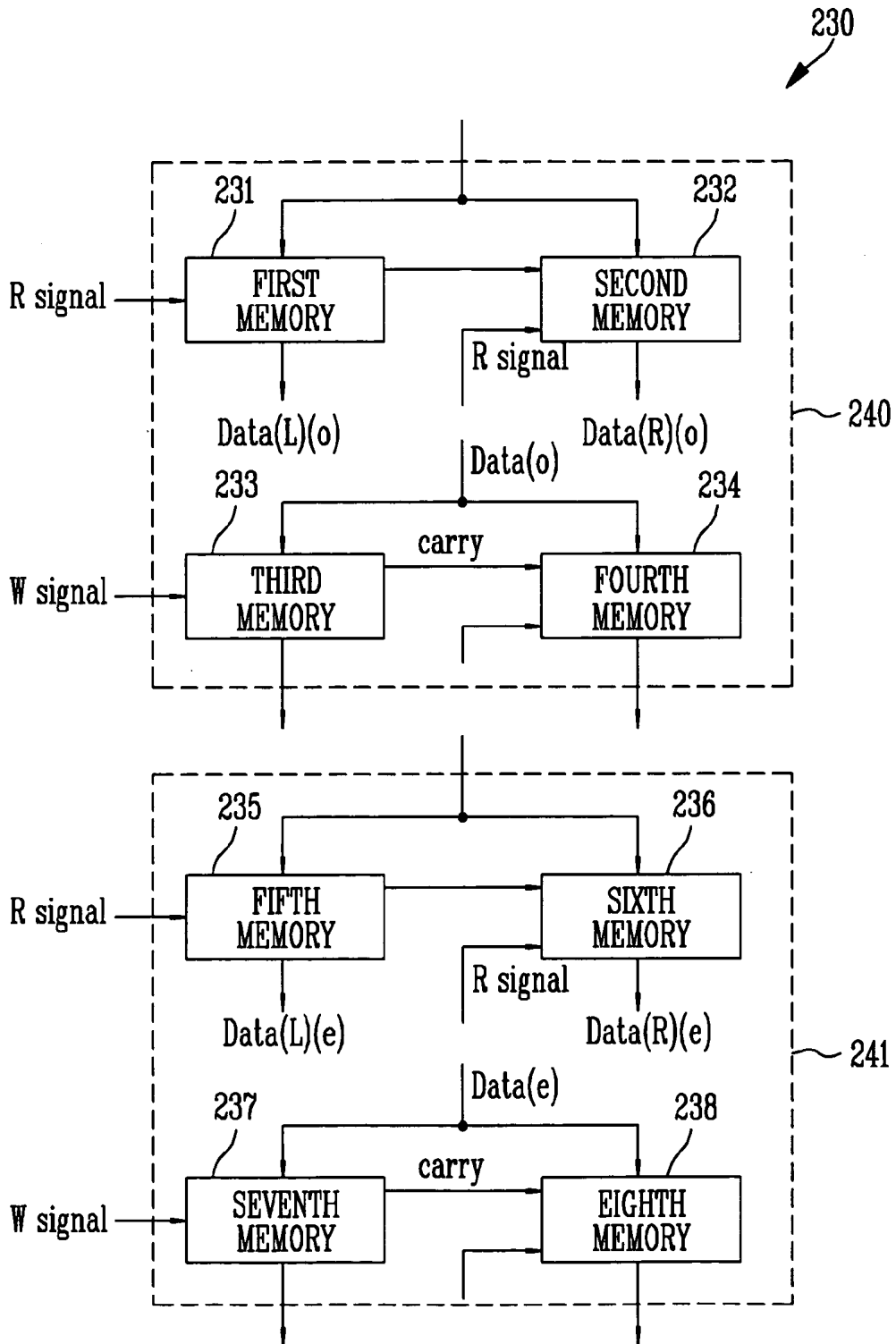


FIG. 8B



ORGANIC LIGHT EMITTING DISPLAY AND METHOD OF DRIVING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2004-0068403, filed on Aug. 30, 2004, in the Korean Intellectual Property Office, the entire content of which is incorporated herein by reference.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates to an organic light emitting display and a method of driving the same, and more particularly, to an organic light emitting display and a method of driving the same, in which a driving frequency is lowered and at the same time a production cost is reduced.

[0004] 2. Discussion of Related Art

[0005] Recently, various flat panel displays have been developed to substitute for a cathode ray tube (CRT) display because the CRT display is relatively heavy and bulky. The flat panel display includes a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), and an organic light emitting display.

[0006] Among the flat panel displays, the organic light emitting display can emit light for itself by electron-hole recombination. Such an organic light emitting display has advantages in that response time is relatively fast and power consumption is relatively low. Generally, the organic light emitting display employs a thin film transistor (TFT) provided in each pixel for supplying a current corresponding to a data signal to a light emitting device, thereby allowing the light emitting device to emit light.

[0007] FIG. 1 illustrates a conventional organic light emitting display.

[0008] Referring to FIG. 1, a conventional organic light emitting display includes a display region 30 having a plurality of pixels 1 formed adjacent to respective regions where a plurality of scan lines S1 through Sn and a plurality of data lines D1 through Dm crossed each other, where n and m are natural numbers; a scan driver 20 adapted to drive the scan lines S1 through Sn; a data driver 10 adapted to drive the data lines D1 through Dm; and a controller 40 adapted to control the scan driver 20 and the data driver 10.

[0009] The scan driver 20 generates a scan signal(s) for driving the scan lines S1 through Sn in response to a scan control signal(s) GCS transmitted from the controller 40, and supplies the scan signals to the scan lines S1 through Sn in sequence.

[0010] The data driver 10 receives data control signals DCS and data Data from the controller 40. Then, the data driver 10 is controlled by the data control signals DCS to convert the data Data into voltage (or current), thereby outputting a data signal(s) to the data lines D1 through Dm. At this time, the data driver 10 supplies the data signal corresponding to one horizontal line per horizontal period to the data lines D1 through Dm.

[0011] In operation, a pixel 1 is selected when a scan signal is transmitted to a scan line S, and emits light corresponding to a data signal transmitted to a data line D. For this, each pixel 1 includes at least one switching device and a capacitor.

[0012] The controller 40 generates the data control signals DCS and the scan control signal(s) GCS in response to external synchronization signals. Here, the data control signals DCS are transmitted to the data driver 10, and the scan control signal GCS is transmitted to the scan driver 20.

[0013] Further, the controller 40 temporarily stores external data Data, and supplies the stored data Data to the data driver 10. For this, the controller 40 includes line memories 42 and 44 as shown in FIG. 2A. Additionally, the temporarily stored data Data can be supplied to a gamma generator (not shown). Then, the gamma generator generates the data signal in response to a gradation level of the data Data, and supplies the data signal to the data driver 10.

[0014] FIGS. 2A and 2B illustrate line memories provided in a controller of a conventional organic light emitting display.

[0015] Referring to FIGS. 2A and 2B, the controller 40 includes the first line memory 42 and the second line memory 44. Each of the line memories 42 and 44 is set to have a certain capacity to store data corresponding to one horizontal line. Here, the first line memory 42 and the second line memory 44 repeatedly alternate between writing and reading operations, alternately.

[0016] For example, as shown in FIG. 2A, while a writing signal W is transmitted to the first line memory 42, a reading signal R is transmitted to the second line memory 44. Here, the writing signal W and the reading signal R include various signals such as an address signal, a clock signal, etc. When the writing signal W is transmitted to the first line memory 42, the first line memory 42 stores external data Data corresponding to one horizontal line in sequence. Further, when the reading signal R is transmitted to the second line memory 44, the second line memory 44 supplies the data Data stored therein corresponding to one horizontal line to the data driver 10.

[0017] On the other hand, as shown in FIG. 2B, while the reading signal R is transmitted to the first line memory 42, the writing signal W is transmitted to the second line memory 44. When the reading signal R is transmitted to the first line memory 42, the first line memory 42 supplies the data Data stored therein corresponding to one horizontal line to the data driver 10. Further, when the writing signal W is transmitted to the second line memory 44, the second line memory 44 stores the external data Data corresponding to one horizontal line in sequence.

[0018] That is, the conventional organic light emitting display shown in FIG. 1 employs the line memories 42 and 44 to temporarily store the data Data and supply the stored data Data to the data driver 10, thereby displaying a predetermined image. Here, the line memories 42 and 44 store a plurality of data Data and supply the stored data Data to the data driver 10 per one horizontal period 1H, so that the reading signal R and the writing signal W have a high clock frequency.

[0019] Thus, because the clocks included in the reading signal R and the writing signal W have high frequency, an

electromagnetic interference (EMI) or the like is generated, thereby deteriorating a driving operation of the organic light emitting display. Further, because each of the reading signal R and the writing signal W has the high clock frequency, a need arises for a high performance integrated circuit (IC) which can be stably driven at the high frequency, and thus a problem arises in that a production cost is increased. To solve this problem, there has been proposed an organic light emitting display as shown in FIG. 3.

[0020] FIG. 3 illustrates another conventional organic light emitting display. In FIG. 3, like numerals as those in FIG. 1 refer to like elements, and descriptions for elements that are substantially similar to those described above for the display of FIG. 1 will be avoided.

[0021] Referring to FIG. 3, the organic light emitting display includes a display region 30 having a plurality of pixels 1 formed adjacent to respective regions where a plurality of scan lines S1 through Sn and a plurality of data lines D1 through Dm crossed each other, where n and m are natural numbers; a scan driver 20 adapted to drive the scan lines S1 through Sn; a first data driver 12 adapted to drive odd numbered data lines D1, D3, . . . , Dm-1; a second data driver 14 adapted to drive even numbered data lines D2, D4, . . . , Dm; and a controller 50 adapted to control the scan driver 20, the first data driver 12, and the second data driver 14.

[0022] The scan driver 20 generates a scan signal(s) for driving the scan lines S1 through Sn in response to a scan control signal(s) GCS transmitted from the controller 50, and supplies the scan signals to the scan lines S1 through Sn in sequence.

[0023] The first data driver 12 receives data control signals DCS and odd numbered data Data(o) from the controller 50. Then, the first data driver 12 is controlled by the data control signals DCS to convert the odd numbered data Data(o) into voltage (or current), thereby outputting an odd numbered data signal(s) to the odd numbered data lines D1, D3, . . . , Dm-1. At this time, the first data driver 12 supplies the odd numbered data signal(s) corresponding to one horizontal line per horizontal period to the odd numbered data lines D1, D3, . . . , Dm-1.

[0024] In addition, the second data driver 14 receives the data control signals DCS and even numbered data Data(e) from the controller 50. Then, the second data driver 14 is controlled by the data control signals DCS to convert the even numbered data Data(e) into voltage (or current), thereby outputting an even numbered data signal(s) to the even numbered data lines D2, D4, . . . , Dm. At this time, the second data driver 14 supplies the even numbered data signal(s) corresponding to one horizontal line per horizontal period to the even numbered data lines D2, D4, . . . , Dm.

[0025] In operation, a pixel 1 is selected when a scan signal is transmitted to a scan line S, and emits light corresponding to a data signal transmitted to a data line D. For this, each pixel 1 includes at least one switching device and a capacitor.

[0026] The controller 50 generates the data control signals DCS and the scan control signal(s) GCS in response to external synchronization signals. Here, the data control signals DCS are transmitted to the first and second data

drivers 12 and 14, and the scan control signal GCS is transmitted to the scan driver 20.

[0027] Further, the controller 50 temporarily stores external data Data as the odd numbered data Data(o) and the even numbered data Data(e), and supplies the stored odd numbered data Data(o) and the stored even numbered data Data(e) to the first and second data drivers 12 and 14, respectively. For this, the controller 50 includes line memory blocks 53 and 56 as shown in FIG. 4A. Additionally, the temporarily stored data Data can be supplied from the controller 50 to a gamma generator (not shown). Then, the gamma generator generates the data signal in response to a gradation level of the data Data, and supplies the data signal to the first and second data drivers 12 and 14.

[0028] FIGS. 4A and 4B illustrate line memories provided in a controller of a conventional organic light emitting display.

[0029] Referring to FIGS. 4A and 4B, the controller 50 includes the first line memory block 53 and the second line memory block 56. The first line memory block 53 includes a first memory 51 and a second memory 52. Each of the first and second memories 51 and 52 is set to have a certain capacity to store data corresponding to a half horizontal line. Here, the first memory 51 and the second memory 52 repeatedly alternate between writing and reading operations. Further, the second memory block 56 includes a third memory 54 and a fourth memory 55. Each of the third and fourth memories 54 and 55 is set to have a certain capacity to store data corresponding to a half horizontal line. Here, the third memory 54 and the fourth memory 55 repeatedly alternate between writing and reading operations.

[0030] For example, as shown in FIG. 4A, while a writing signal W is transmitted to the first and third memories 51 and 54, a reading signal R is transmitted to the second and fourth memories 52 and 55. When the writing signal W is transmitted to the first memory 51, the first memory 51 stores external odd numbered data Data(o) corresponding to one horizontal line in sequence. Further, when the writing signal W is transmitted to the third memory 54, the third memory 54 stores external even numbered data Data(e) corresponding to one horizontal line in sequence.

[0031] When the reading signal R is transmitted to the second memory 52, the second memory 52 supplies the odd numbered data Data(o) stored therein corresponding to one horizontal line to the first data driver 12. Here, the second memory 52 either outputs the odd numbered data Data(o) at the same time or in sequence. When the reading signal R is transmitted to the fourth memory 55, the fourth memory 55 supplies the even numbered data Data(e) stored therein corresponding to one horizontal line to the second data driver 14. Here, the fourth memory 55 either outputs the odd numbered data Data(e) at the same time or in sequence.

[0032] On the other hand, as shown in FIG. 4B, while the reading signal R is transmitted to the first and third memories 51 and 54, the writing signal W is transmitted to the second and fourth memories 52 and 55. When the reading signal R is transmitted to the first memory 51, the first memory 51 supplies the odd numbered data Data(o) stored therein for a previous horizontal period to the first data driver 12. When the reading signal R is transmitted to the third memory 54, the third memory 54 supplies the even

numbered data Data(e) stored therein for the previous horizontal period to the second data driver 14.

[0033] When the writing signal W is transmitted to the second memory 52, the second memory 52 stores the external odd numbered data Data(o) therein corresponding to one horizontal line in sequence. When the writing signal W is transmitted to the fourth memory 55, the fourth memory 55 stores the even numbered data Data(e) therein corresponding to one horizontal line in sequence.

[0034] Thus, each of the conventional memories 51, 52, 54 and 55 stores odd or even numbered data Data(o) or Data(e), and supplies the stored odd or even numbered data Data(o) or Data(e) to the first data driver or the second data driver 12 or 14, so that the frequency of the clock included in the reading and writing signals R and W can be advantageously lowered by about half as compared with the organic light emitting display of FIG. 1. However, the conventional organic light emitting display of FIG. 3 is in need of different data drivers 12 and 14 to drive the odd numbered data lines D1, D3, . . . , Dm-1 and the even numbered data lines D2, D4, . . . , Dm, so that the picture quality may be deteriorated.

[0035] In more detail, the first data driver 12 and the second data driver 14 have to supply the odd numbered data signal and the even numbered data signal at the same time. However, the data control signals DCS are not transmitted to the first and second data drivers 12 and 14 at the same time due to line resistance or the like, and thus the odd numbered data signal and the even numbered data signal are transmitted at different times. Because as the odd numbered data signal and the even numbered data signal are not supplied at the same time, the picture quality is deteriorated by a unit of a vertical line.

[0036] Further, the odd numbered data lines D1, D3, . . . , Dm-1 and the even numbered data lines D2, D4, . . . , Dm are driven by the different data drivers 12 and 14, so that interference arises due to a capacitance equivalently formed between adjacent data lines D, and the picture quality may be further deteriorated.

SUMMARY OF THE INVENTION

[0037] Accordingly, an embodiment of the present invention provides an organic light emitting display and a method of driving the same, in which a driving frequency is lowered and at the same time a production cost is reduced.

[0038] One embodiment of the present invention provides an organic light emitting display including: a display region divided into a left part and a right part; a first data driver adapted to supply a data signal to data lines of the left part; a second data driver adapted to supply a data signal to data lines of the right part; and first and second memory groups, wherein, when one of the first and second memory groups stores data to be supplied to the left and right parts therein, another one of the first and second memory groups supplies data to the first and second data drivers, and, wherein, when one of the first and second memory groups receives a reading signal in parallel, another one of the first and second memory groups receives a writing signal in series.

[0039] One embodiment of the present invention provides an organic light emitting display including: a display region divided into a left part and a right part; a first data driver

adapted to supply a data signal to data lines corresponding to the left part; a second data driver adapted to supply the data signal to data lines corresponding to the right part; first and third memories, wherein, when one of the first and third memories stores data to be supplied to the left part, another one of the first and third memories supplies data stored therein for the left part to the first data driver; and second and fourth memories, wherein, when one of the second and fourth memories stores data to be supplied to the right part, another one of the second and fourth memories supplies data stored therein for the right part to the second data driver, wherein a reading signal is supplied to one of the first and third memories and one of the second and fourth memories at the same time.

[0040] One embodiment of the present invention provides an organic light emitting display including: a display region divided into a left part and a right part; a first data driver adapted to supply a data signal to odd numbered data lines corresponding to the left part; a second data driver adapted to supply the data signal to odd numbered data lines corresponding to the right part; a third data driver adapted to supply the data signal to even numbered data lines corresponding to the left part; a fourth data driver adapted to supply the data signal to even numbered data lines corresponding to the right part; a first line memory block adapted to store odd numbered data to be supplied to the left and right parts in sequence in response to a writing signal and to output odd numbered data stored therein for the left and right parts at the same time in response to a reading signal; and a second line memory block adapted to store even numbered data to be supplied to the left and right parts in sequence in response to the writing signal and to output even numbered data stored therein for the left and right parts at the same time in response to the reading signal.

[0041] One embodiment of the present invention provides a method of driving an organic light emitting display. The method includes: storing data to be supplied to a left part of a display region in a first memory in response to a writing signal; storing data to be supplied to a right part of the display region in a second memory in response to a carry signal supplied from the first memory after the first memory stores the data to be supplied to the left part; and outputting the data stored in the first memory and the data stored in the second memory by transmitting a reading signal to the first memory and the second memory at the same time.

[0042] One embodiment of the present invention provides a method of driving an organic light emitting display having a display region divided into a left part and a right part. The method includes: storing odd numbered data to be supplied to the left part in a first memory in response to a writing signal; storing odd numbered data to be supplied to the right part in a second memory in response to a carry signal supplied from the first memory after the first memory stores the odd numbered data for the left part; storing even numbered data to be supplied to the left part in a third memory in response to a writing signal; storing even numbered data to be supplied to the right part in a fourth memory in response to a carry signal supplied from the third memory after the third memory stores the even numbered data for the left part; and outputting the data stored in the first, second, third, and fourth memories by transmitting a reading signal to the first, second, third, and fourth memories, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

[0043] The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention, and, together with the description, serve to explain the principles of the present invention.

[0044] FIG. 1 illustrates a conventional organic light emitting display;

[0045] FIGS. 2A and 2B illustrate line memories provided in a controller of FIG. 1;

[0046] FIG. 3 illustrates another conventional organic light emitting display;

[0047] FIGS. 4A and 4B illustrate line memories provided in a controller of FIG. 3;

[0048] FIG. 5 illustrates an organic light emitting display according to a first embodiment of the present invention;

[0049] FIGS. 6A and 6B illustrate line memories provided in a controller of FIG. 5;

[0050] FIG. 7 illustrates an organic light emitting display according to a second embodiment of the present invention; and

[0051] FIGS. 8A and 8B illustrate line memories provided in a controller of FIG. 7.

DETAILED DESCRIPTION

[0052] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. The exemplary embodiments of the present invention are provided to be readily understood by those skilled in the art.

[0053] FIG. 5 illustrates an organic light emitting display according to a first embodiment of the present invention.

[0054] Referring to FIG. 5, the organic light emitting display according to the first embodiment of the present invention includes a display region 120 having a plurality of pixels 140 formed adjacent to respective regions where a plurality of scan lines S1 through Sn and a plurality of data lines D1 through Dm crossed each other, where n and m are natural numbers; a scan driver 110 adapted to drive the scan lines S1 through Sn; first and second data drivers 100 and 101 adapted to drive the data lines D1 through Dm; and a controller 130 adapted to control the scan driver 110 and the first and second data drivers 100 and 101.

[0055] The scan driver 110 generates a scan signal(s) for driving the scan lines S1 through Sn in response to a scan control signal(s) GCS transmitted from the controller 130, and supplies the scan signals to the scan lines S1 through Sn in sequence.

[0056] In operation, a pixel 140 is selected when a scan signal is transmitted to a scan line S, and emits light corresponding to a data signal transmitted to a data line D. For this, each pixel 140 includes at least one switching device and a capacitor.

[0057] A display region 120 includes the plurality of pixels 140. Further, the display region 120 is driven as it is divided into a left part 122 and a right part 124. The left part 122 includes a first data line D1 through the i^{th} data line Di,

where i is $m/2$. The right part 124 includes the $(i+1)^{\text{th}}$ data line Di+1 through the m^{th} data line Dm.

[0058] The first and second data drivers 100 and 101 receive data control signals DCS and data Data from the controller 130. Then, the first and second data drivers 100 and 101 are controlled by the data control signals DCS to convert the data Data into voltage (or current), thereby outputting a data signal(s) to the data lines D1 through Dm. At this time, the first data driver 100 supplies the data signal to the first data line D1 through the i^{th} data line Di included in the left part 122, and the second data driver 101 supplies the data signal to the $(i+1)^{\text{th}}$ data line Di+1 through the m^{th} data line Dm included in the right part 124.

[0059] The controller 130 generates the data control signals DCS and the scan control signal(s) GCS in response to external synchronization signals. Here, the data control signals DCS are transmitted to the first and second data drivers 100 and 101, and the scan control signal GCS is transmitted to the scan driver 110.

[0060] Further, the controller 130 temporarily stores external data Data, and supplies the stored data Data (L) and Data (R) to the first and second data drivers 100 and 101. For this, the controller 130 includes line memory blocks 135 and 136 as shown in FIG. 6A. Additionally, the temporarily stored data Data can be supplied from the controller 130 to a gamma generator (not shown). Then, the gamma generator generates the data signal in response to a gradation level of the data Data, and supplies the data signal to the first and second data drivers 100 and 101. In this embodiment, the memory blocks 135 and 136 are provided in the controller 130 for exemplary purpose and the present invention is not thereby limited. For example, in one embodiment, the memory blocks are provided outside the controller 130.

[0061] FIGS. 6A and 6B illustrate line memory blocks provided in a controller of FIG. 5.

[0062] Referring to FIGS. 6A and 6B, the controller 130 includes the first line memory block 135 and the second line memory block 136. The first line memory block 135 includes a first memory 131 and a second memory 132. Each of the first and second memories 131 and 132 is set to have a certain capacity to store data corresponding to a half horizontal line. In other words, the capacity of the first memory 131 is set to store the data Data(L) to be supplied to the left part 122 of the display region 120, and the capacity of the second memory 132 is set to store the data Data(R) to be supplied to the right part 124 of the display region 120.

[0063] The second line memory block 136 includes a third memory 133 and a fourth memory 134. Each of the third and fourth memories 133 and 134 is set to have capacity to store data corresponding to a half horizontal line. In other words, the capacity of the third memory 133 is set to store the data Data(L) to be supplied to the left part 122, and the capacity of the fourth memory 134 is set to store the data Data(R) to be supplied to the right part 124. Here, the first and second memories 131 and 132, and the third and fourth memories 133 and 134 repeatedly alternate between reading and writing operations.

[0064] For example, as shown in FIG. 6A, while a writing signal W is transmitted to the first memory 131, a reading signal R is transmitted to the third and fourth memories 133

and 134. Here, the writing signal W and the reading signal R include various signals such as an address signal, a clock signal, etc. When the writing signal W is transmitted to the first memory 131, the first memory 131 stores data Data(L) to be supplied to the left part 122 of external data Data in sequence. When the first memory 131 completely stores the data Data(L) to be supplied to the left part 122, the first memory 131 transmits a carry signal to the second memory 132. After receiving the carry signal, the second memory 132 stores data Data(R) to be supplied to the right part 124 of the external data Data in sequence. In FIG. 6A, the writing signal W is supplied to the first line memory block 135 in series.

[0065] When the reading signal R is transmitted to the third memory 133, the third memory 133 supplies the data Data(L) stored therein for the left part 122 to the first data driver 100. Here, the third memory 133 either outputs the data Data(L) for the left part 122 at the same time or in sequence. Further, when the reading signal R is transmitted to the fourth memory 134, the fourth memory 134 supplies the data Data(R) stored therein for the right part 124 to the second data driver 101. Here, the fourth memory 134 either outputs the data Data(R) for the right part 124 at the same time or in sequence. In FIG. 6A, the reading signal R is supplied to the second line memory block 136 in parallel.

[0066] Then, as shown in FIG. 6B, while the reading signal R is transmitted to the first and second memories 131 and 132, the writing signal W is transmitted to the third memory 133. When the reading signal R is transmitted to the first memory 131, the first memory 131 supplies the data Data(L) stored during a previous horizontal period for the left part 122 to the first data driver 100. Here, the first memory 131 either outputs the data Data(L) for the left part 122 at the same time or in sequence. Further, when the reading signal R is transmitted to the second memory 132, the second memory 132 supplies the data Data(R) stored therein for the right part 124 to the second data driver 101. Here, the second memory 132 either outputs the data Data(R) for the right part 124 at the same time or in sequence. In FIG. 6B, the reading signal R is supplied to the first line memory block 135 in parallel.

[0067] When the writing signal W is transmitted to the third memory 133, the third memory 133 stores data Data(L) to be supplied to the left part 122 of the external data Data in sequence. When the third memory 133 completely stores the data Data(L) to be supplied to the left part 122, the third memory 133 transmits the carry signal to the fourth memory 134. After receiving the carry signal, the fourth memory 134 stores data Data(R) to be supplied to the right part 124 of the external data Data in sequence. In FIG. 6B, the writing signal W is supplied to the second line memory block 136 in series.

[0068] According to the first embodiment of the present invention, the reading signal R clock is supplied to the memories provided in each line memory blocks 135 and 136 in parallel (or at the same time), and the writing signal W clock is supplied to the memories provided in each line memory blocks 135 and 136 in series. Thus, the reading signal R clock is supplied to the memories provided in each line memory blocks 135 and 136, so that the frequency of the clock included in reading signal R can be advantageously lowered by about half as compared with the conventional organic light emitting display of FIG. 1.

[0069] Accordingly, as the frequency of the clock included in reading signal R can be advantageously lowered by about half as compared with the conventional organic light emitting display, an electromagnetic interference (EMI) is decreased. Further, accordingly, as the frequency of the clock included in reading signal R can be advantageously lowered by about half as compared with the conventional organic light emitting display, it is possible to employ an integrated chip (IC) or the like operating in low frequency, thereby reducing a production cost of the organic light emitting display. According to the first embodiment of the present invention, the display region 120 is divided into the left part 122 and the right part 124, so that the picture quality is prevented from being deteriorated by a unit of a vertical line, and at the same time an interference between adjacent data lines D due to a capacitance effect is minimized.

[0070] FIG. 7 illustrates an organic light emitting display according to a second embodiment of the present invention.

[0071] Referring to FIG. 7, the organic light emitting display according to the second embodiment of the present invention includes a display region 220 having a plurality of pixels 250 formed adjacent to respective regions where a plurality of scan lines S1 through Sn and a plurality of data lines D1 through Dm crossed each other, where n and m are natural numbers; a scan driver 210 adapted to drive the scan lines S1 through Sn; first, second, third, and fourth data drivers 200, 201, 202, and 203 to drive the data lines D1 through Dm; and a controller 230 adapted to control the scan driver 210 and the first through fourth data drivers 200 through 203.

[0072] The scan driver 210 generates a scan signal(s) for driving the scan lines S1 through Sn in response to a scan control signal(s) GCS transmitted from the controller 230, and supplies the scan signals to the scan lines S1 through Sn in sequence.

[0073] In operation, a pixel 250 is selected when a scan signal is transmitted to a scan line S, and emits light corresponding to a data signal transmitted to a data line D. For this, each pixel 250 includes at least one switching device and a capacitor.

[0074] A display region 220 includes the plurality of pixels 250. Further, the display region 220 is driven as it is divided into a left part 222 and a right part 224. The left part 222 includes a first data line D1 through the ith data line Di. The right part 224 includes the (i+1)th data line Di+1 through the mth data line Dm.

[0075] The first data driver 200 receives data control signals DCS and odd numbered data Data (L)(o) for the left part 222 from the controller 230. The second data driver 201 receives the data control signals DCS and odd numbered data Data (R)(o) for the right part 224 from the controller 230. The third data driver 202 receives the data control signals DCS and even numbered data Data (L)(e) for the left part 222 from the controller 230. The fourth data driver 203 receives the data control signals DCS and even numbered data Data (R)(e) for the right part 224 from the controller 230.

[0076] The first through fourth data drivers 200 through 203 are controlled by the data control signals DCS to convert the data Data into voltage (or current), thereby outputting a data signal(s) to the data lines D1 through Dm. At this time,

the first through fourth data drivers **200** through **203** supply the data signal to the data lines D1 through Dm per one horizontal period.

[**0077**] The controller **230** generates the data control signals DCS and the scan control signal(s) GCS in response to external synchronization signals. Here, the data control signals DCS are transmitted to the first through fourth data drivers **200** through **203**, and the scan control signal GCS is transmitted to the scan driver **210**.

[**0078**] Further, the controller **230** temporarily stores external data Data, and supplies the stored data Data (L)(o), Data (R)(o), Data (L)(e), and Data (R)(e) to the first through fourth data drivers **200** through **203**. For this, the controller **230** includes line memory blocks **240** and **241** as shown in **FIG. 8A**. Additionally, the temporarily stored data Data can be supplied from the controller **230** to a gamma generator (not shown). Then, the gamma generator generates the data signal in response to a gradation level of the data Data, and supplies the data signal to the first through fourth data drivers **200** through **203**. In this embodiment, the line memory blocks **240** and **241** are provided in the controller **230** for exemplary purposes and the present invention is not thereby limited. For example, in one embodiment, the memory blocks are provided outside the controller **230**.

[**0079**] **FIGS. 8A and 8B** illustrate line memory blocks provided in a controller of **FIG. 7**.

[**0080**] Referring to **FIGS. 8A and 8B**, the controller **230** includes the first line memory block **240** and the second line memory block **241**. The first line memory block **240** includes a first memory **231**, a second memory **232**, a third memory **233**, and a fourth memory **234**. Each of the first through fourth memories **231** through **233** is set to have a certain capacity to store data corresponding to a quarter horizontal line. In other words, the capacity of each of the first and third memories **231** and **233** is set to store the odd numbered data Data(L)(o) for the left part **222**, and the capacity of each of the second and fourth memories **232** and **234** is set to store the odd numbered data Data(R)(o) for the right part **224**.

[**0081**] The second line memory block **241** includes a fifth memory **235**, a sixth memory **236**, a seventh memory **237**, and an eighth memory **238**. Each of the fifth through eighth memories **235** through **238** is set to have a certain capacity to store data corresponding to a quarter horizontal line. In other words, the capacity of each of the fifth and seventh memories **235** and **237** is set to store the even numbered data Data(L)(e) for the left part **222**, and the capacity of each of the sixth and eighth memories **236** and **238** is set to store the even numbered data Data(R)(e) for the right part **224**.

[**0082**] For example, as shown in **FIG. 8A**, while a writing signal W is transmitted to the first and fifth memories **231** and **235**, a reading signal R is transmitted to the third, fourth, seventh and eighth memories **233**, **234**, **237** and **238**. When the writing signal W is transmitted to the first memory **231**, the first memory **231** stores the odd numbered data Data(L)(o) for the left part **222** of external data Data in sequence. When the first memory **231** completely stores the odd numbered data Data(L)(o) for the left part **222**, the first memory **231** transmits a carry signal to the second memory **232**. After receiving the carry signal, the second memory **232** stores the odd numbered data Data(R)(o) for the right part **224** of the external data Data in sequence.

[**0083**] When the writing signal W is transmitted to the fifth memory **235**, the fifth memory **235** stores the even numbered data Data(L)(e) for the left part **222** of the external data Data in sequence. When the fifth memory **235** completely stores the even numbered data Data(L)(e) for the left part **222**, the fifth memory **235** transmits a carry signal to the sixth memory **236**. After receiving the carry signal, the sixth memory **236** stores the even numbered data Data(R)(e) for the right part **224** of the external data Data in sequence.

[**0084**] When the reading signal R is transmitted to the third memory **233**, the third memory **233** supplies the odd numbered data Data(L)(o) stored therein for the left part **222** to the first data driver **200**. Here, the third memory **233** either outputs the odd numbered data Data(L)(o) for the left part **222** at the same time or in sequence.

[**0085**] When the reading signal R is transmitted to the fourth memory **234**, the fourth memory **234** supplies the odd numbered data Data(R)(o) stored therein for the right part **224** to the second data driver **201**. Here, the fourth memory **234** either outputs the odd numbered data Data(R)(o) for the right part **224** at the same time or in sequence.

[**0086**] When the reading signal R is transmitted to the seventh memory **237**, the seventh memory **237** supplies the even numbered data Data(L)(e) stored therein for the left part **222** to the third data driver **202**. Here, the seventh memory **237** either outputs the even numbered data Data(L)(e) for the left part **222** at the same time or in sequence.

[**0087**] When the reading signal R is transmitted to the eighth memory **238**, the eighth memory **238** supplies the even numbered data Data(R)(e) stored therein for the right part **224** to the fourth data driver **203**. Here, the eighth memory **238** either outputs the even numbered data Data(R)(e) for the right part **224** at the same time or in sequence.

[**0088**] Then, as shown in **FIG. 8B**, while the reading signal R is transmitted to the first, second, fifth and sixth memories **231**, **232**, **235** and **236**, the writing signal W is transmitted to the third and seventh memories **233** and **237**.

[**0089**] When the writing signal W is transmitted to the third memory **233**, the third memory **233** stores the odd numbered data Data(L)(o) for the left part **222** of external data Data in sequence. When the third memory **233** completely stores the odd numbered data Data(L)(o) for the left part **222**, the third memory **233** transmits the carry signal to the fourth memory **234**. After receiving the carry signal, the fourth memory **234** stores the odd numbered data Data(R)(o) for the right part **224** of the external data Data in sequence.

[**0090**] When the writing signal W is transmitted to the seventh memory **237**, the seventh memory **237** stores the even numbered data Data(L)(e) for the left part **222** of the external data Data in sequence. When the seventh memory **237** completely stores the even numbered data Data(L)(e) for the left part **222**, the seventh memory **237** transmits the carry signal to the eighth memory **238**. After receiving the carry signal, the eighth memory **238** stores the even numbered data Data(R)(e) for the right part **224** of the external data Data in sequence.

[**0091**] When the reading signal R is transmitted to the first memory **231**, the first memory **231** supplies the odd num-

bered data Data(L)(o) stored therein for the left part 222 to the first data driver 200. Here, the first memory 231 either outputs the odd numbered data Data(L)(o) for the left part 222 at the same time or in sequence.

[0092] When the reading signal R is transmitted to the second memory 232, the second memory 232 supplies the odd numbered data Data(R)(o) stored therein for the right part 224 to the second driver 201. Here, the second memory 232 either outputs the odd numbered data Data(R)(o) for the right part 224 at the same time or in sequence.

[0093] When the reading signal R is transmitted to the fifth memory 235, the fifth memory 235 supplies the even numbered data Data(L)(e) stored therein for the left part 222 to the third data driver 202. Here, the fifth memory 235 either outputs the even numbered data Data(L)(e) for the left part 222 at the same time or in sequence.

[0094] When the reading signal R is transmitted to the sixth memory 236, the sixth memory 236 supplies the even numbered data Data(R)(e) stored therein for the right part 224 to the fourth data driver 203. Here, the sixth memory 236 either outputs the even numbered data Data(R)(e) for the right part 224 at the same time or in sequence.

[0095] According to the second embodiment of the present invention, the display region 220 is driven as it is divided into the left part 222 and the right part 224. Further, according to the second embodiment of the present invention, the data line D is driven as it is divided into the odd numbered data lines D1, D3, . . . , Dm-1, and the even numbered data lines D2, D4, . . . , Dm.

[0096] Here, the first memory 231 and the third memory 233 store the odd numbered data Data(L)(o) therein for the left part 222 and supply the stored odd numbered data Data(L)(o) to the left part 222. The fifth memory 235 and the seventh memory 237 store the even numbered data Data(L)(e) therein for the left part 222 and supply the stored even numbered data Data(L)(e) to the left part 222. The second memory 232 and the fourth memory 234 store the odd numbered data Data(R)(o) therein for the right part 224 and supply the stored odd numbered data Data(R)(o) to the right part 224. The sixth memory 236 and the eighth memory 238 store the even numbered data Data(R)(e) therein for the right part 224 and supply the stored even numbered data Data(R)(e) to the right part 224.

[0097] Further, the frequency of the writing signal W is set to store the odd numbered data Data(o) or the even numbered data Data(e) in sequence. Thus, the frequency of the clock included in the writing signal W is lowered by about half as compared with the conventional organic light emitting display of FIG. 1. Further, the reading signal R is set to output the odd numbered data for the left part 222, the even numbered data for the left part 222, the odd numbered data for the right part 224, and the even numbered data for the right part 224, which are previously stored in the respective memories. Thus, the frequency of the clock included in the reading signal R is lowered by about a quarter as compared with the conventional organic light emitting display of FIG. 1.

[0098] According to the second embodiment of the present invention, the writing signal W and the reading signal R are set to have relatively low frequency, so that an EMI is decreased. Further, since the writing signal W and the

reading signal R are set to have a relatively low frequency, it is possible to employ an integrated chip (IC) or the like operating in low frequency, thereby reducing a production cost of the organic light emitting display.

[0099] As described above, the present invention provides an organic light emitting display and a method of driving the same, in which data is divided and supplied corresponding to a left part and a right part of a panel, so that the frequency of a clock included in a reading signal supplied to a line memory is lowered, thereby reducing a production cost.

[0100] Further, the present invention provides an organic light emitting display and a method of driving the same, in which data is divided and supplied corresponding to a left part and a right part of a panel and at the same time corresponding to an odd numbered data line and an even numbered data line, so that the frequencies of clocks included in a reading signal and a writing signal supplied to a line memory are lowered, thereby reducing a production cost.

[0101] Although certain embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in these embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.

What is claimed is:

1. An organic light emitting display comprising:

- a display region divided into a left part and a right part;
- a first data driver for supplying a data signal to data lines of the left part;
- a second data driver for supplying the data signal to data lines of the right part; and
- first and second memory groups,

wherein, when one of the first and second memory groups stores data to be supplied to the left and right parts therein, another one of the first and second memory groups supplies data stored therein to the first and second data drivers, and

wherein, when one of the first and second memory groups receives a reading signal in parallel, another one of the first and second memory groups receives a writing signal in series.

2. The organic light emitting display according to claim 1, wherein the first memory group includes a first memory and a second memory, and the second memory group includes a third memory and a fourth memory.

3. The organic light emitting display according to claim 2, wherein the third memory and the fourth memory store the data for the left and right parts in response to the writing signal while the first memory and the second memory supply the data stored therein for the left and right parts to the first and second data drivers in response to the reading signal.

4. The organic light emitting display according to claim 2, wherein the first memory and the second memory store the data for the left and right parts in response to the writing signal while the third memory and the fourth memory supply the data stored therein for the left and right parts to the first and second data drivers in response to the reading signal.

5. An organic light emitting display comprising:
 a display region divided into a left part and a right part;
 a first data driver adapted to supply a data signal to data lines corresponding to the left part;
 a second data driver adapted to supply the data signal to data lines corresponding to the right part;
 first and third memories,
 wherein, when one of the first and third memories stores data to be supplied to the left part, another one of the first and third memories supplies data stored therein for the left part to the first data driver; and
 second and fourth memories,
 wherein, when one of the second and fourth memories stores data to be supplied to the right part, another one of the second and fourth memories supplies data stored therein for the right part to the second data driver,
 wherein a reading signal is supplied to one of the first and third memories and one of the second and fourth memories at the same time.
6. The organic light emitting display according to claim 5, wherein a writing signal is supplied to the third memory while the reading signal is supplied to the first memory and the second memory.
7. The organic light emitting display according to claim 6, wherein the third memory supplies a carry signal to the fourth memory after storing the data for the left part, and then the fourth memory stores the data for the right part in response to the carry signal.
8. The organic light emitting display according to claim 5, wherein the writing signal is supplied to the first memory while the reading signal is supplied to the third memory and the fourth memory.
9. The organic light emitting display according to claim 8, wherein the first memory supplies a carry signal to the second memory after storing the data for the left part, and then the second memory stores the data for the right part in response to the carry signal.
10. The organic light emitting display according to claim 6, wherein a clock frequency of the reading signal is set to be lower than a clock frequency of the writing signal.
11. The organic light emitting display according to claim 8, wherein the clock frequency of the reading signal is set to be lower than a clock frequency of the writing signal.
12. An organic light emitting display comprising:
 a display region divided into a left part and a right part;
 a first data driver adapted to supply a data signal to odd numbered data lines corresponding to the left part;
 a second data driver adapted to supply the data signal to odd numbered data lines corresponding to the right part;
 a third data driver adapted to supply the data signal to even numbered data lines corresponding to the left part;
 a fourth data driver adapted to supply the data signal to even numbered data lines corresponding to the right part;
 a first line memory block adapted to store odd numbered data to be supplied to the left and right parts in sequence in response to a writing signal and to output odd numbered data stored therein for the left and right parts at the same time in response to a reading signal; and
 a second line memory block adapted to store even numbered data to be supplied to the left and right parts in sequence in response to the writing signal and to output even numbered data stored therein for the left and right parts at the same time in response to the reading signal.
13. The organic light emitting display according to claim 12, wherein the first line memory block comprises:
 first and third memories adapted to store the odd numbered data for the left part in response to the writing signal and to supply the odd numbered data for the left part to the first data driver in response to the reading signal; and
 second and fourth memories adapted to store the odd numbered data for the right part in response to a carry signal respectively supplied from the first memory and the third memory and to supply the odd numbered data for the right part to the second data driver in response to the reading signal.
14. The organic light emitting display according to claim 12, wherein the second line memory block comprises:
 fifth and seventh memories adapted to store the even numbered data for the left part in response to the writing signal and to supply the even numbered data for the left part to the third data driver in response to the reading signal; and
 sixth and eighth memories adapted to store the even numbered data for the right part in response to a carry signal respectively supplied from the fifth memory and the seventh memory and to supply the even numbered data for the right part to the fourth data driver in response to the reading signal.
15. The organic light emitting display according to claim 12, wherein a clock frequency of the reading signal is set to be lower than a clock frequency of the writing signal.
16. A method of driving an organic light emitting display, the method comprising:
 storing data to be supplied to a left part of a display region in a first memory in response to a writing signal;
 storing data to be supplied to a right part of the display region in a second memory in response to a carry signal supplied from the first memory after the first memory stores the data to be supplied to the left part; and
 outputting the data stored in the first memory and the data stored in the second memory by transmitting a reading signal to the first memory and the second memory at the same time.
17. The method according to claim 16, wherein each of the first and second memories outputs the data stored therein at the same time when receiving the reading signal.
18. The method according to claim 16, wherein each of the first and second memories outputs the data stored therein in sequence when receiving the reading signal.
19. The method according to claim 16, further comprising:
 allowing a third memory to store and output the data for the left part alternately with the first memory; and

allowing a fourth memory to store and output the data for the right part alternately with the second memory.

20. A method of driving an organic light emitting display comprising a display region divided into a left part and a right part, the method comprising:

storing odd numbered data to be supplied to the left part in a first memory in response to a writing signal;

storing odd numbered data to be supplied to the right part in a second memory in response to a carry signal supplied from the first memory after the first memory stores the odd numbered data for the left part;

storing even numbered data to be supplied to the left part in a third memory in response to a writing signal;

storing even numbered data to be supplied to the right part in a fourth memory in response to a carry signal supplied from the third memory after the third memory stores the even numbered data for the left part; and

outputting the data stored in the first, second, third, and fourth memories by transmitting a reading signal to the first, second, third, and fourth memories, respectively.

21. The method according to claim 20, wherein each of the first, second, third, and fourth memories outputs the data

stored therein at the same time when receiving the reading signal.

22. The method according to claim 20, wherein each of the first, second, third, and fourth memories outputs the data stored therein in sequence when receiving the reading signal.

23. The method according to claim 20, further comprising:

allowing a fifth memory to store and output the odd numbered data for the left part alternately with the first memory;

allowing a sixth memory to store and output the odd numbered data for the right part alternately with the second memory;

allowing a seventh memory to store and output the even numbered data for the left part alternately with the third memory;

allowing an eighth memory to store and output the even numbered data for the right part alternately with the fourth memory.

* * * * *

专利名称(译)	有机发光显示器及其驱动方法		
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摘要(译)

一种有机发光显示器及其驱动方法，其中驱动频率降低并且同时降低了生产成本。有机发光显示器包括：显示区域，分为左侧部分和右侧部分；第一数据驱动器，适于向左侧部分的数据线提供数据信号；第二数据驱动器，适于将数据信号提供给右部分的数据线；第一和第二存储器组，其中，当第一和第二存储器组之一存储要提供给其中的左和右部分的数据时，第一和第二存储器组中的另一个向第一和第二驱动器提供数据，并且其中当第一和第二存储器组中的一个并行接收读取信号时，第一和第二存储器组中的另一个接收串联的写入信号。利用这种配置，降低了提供给存储器的读取信号中包括的时钟频率，从而降低了生产成本。

